DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 31 March 2010, in response to the Office Action mailed 1 December 2009. The applicant's remarks and any amendments to the claims or specification were considered, with the results that follow.

2. The objection to claim 49 has been withdrawn due to the amendments filed 31 March 2010.

3. Claim 49 has been cancelled while new claims 50 and 51 have been added.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 March 2010 has been entered.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramovici (US 6,034,538) in view of Schmit (Incremental Reconfiguration for Pipelined Applications, April 1997, pages 47-55).

As per claim 50, Abramovici teaches a reconfigurable circuit **[reconfigurable hardware 20 (figure 2)]** including a plurality of data processing units **[FPGAs 1-4 (figure 2)]**, an internal state holding circuit **[local memory 24 (figure 2)]** for holding data being processed inside each of the data processing units **[the page manager (PAGMAN 22) includes one or more first-in-first-out (FIFO) buffers for use in controlling storage and transferring inter-page signal values (i.e. storing the output of one page), which are then used by the next page/FPGA processing (column 5, lines 10-21 and figure 3)]**, a memory portion **[local memory 24 (figure 2)]** for storing data provided from outputs of the data processing units **[the FPGAs communicate with the local memory 24 over bus 23, controlled by the page manager 22, which takes output and register values from the FPGAs and provides**

the FPGAs with inputs and configuration information (column 4, lines 8-19 and figure 2)], and data from an output of a first data processing unit of the plurality of data processing units is supplied to the memory portion **[the page manager (PAGMAN 22) includes one or more first-in-first-out (FIFO) buffers for use in controlling storage and transferring inter-page signal values (i.e. storing the output of one page), which are then used by the next page/FPGA processing (column 5, lines 10-21 and figure 3)]** before being supplied to an input of a second data processing unit of the plurality of the units **[a page configuration for a circuit which includes a feed-forward structure, where the outputs of one page loaded into the FPGAs feed the input of the next page loaded into the FPGAs (column 6, lines 31-44 and figure 5A) where the PAGMAN 22 may include one or more FIFO buffers for use in controlling storage and transfer of inter-page signal values between the FPGAs (column 5, lines 3-50)]**.

While Abramovici teaches that each FPGA can provide a number of reconfigurable functions (and thus multiple data processing sub-units) it does not explicitly teach wherein data from an output of a first data processing sub-unit of the multiple data processing sub-units is supplied to the internal state holding circuit before being supplied to an input of a second data processing sub-unit of the multiple data processing sub-units.

Schmit teaches a data processing unit of the plurality of the units includes multiple data processing sub-units **[a striped FPGA (the data processing unit) consisting of a number (11 in the figure) of stripes (i.e. sub-units) (page 48, figure**

1), where each stripe includes a number of cells (page 54, figure 11)], wherein data from an output of a first data processing sub-unit of the multiple data processing sub-units is supplied to the internal state holding circuit **[immediate results of each stripe/pipeline stage are stored within the cells of that stage (page 52, first paragraph) such as within dedicated memory cells/registers (page 54, section 5.0)]** before being supplied to an input of a second data processing sub-unit of the multiple data processing sub-units **[immediate results of each stripe/pipeline stage may be stored within the cells of that stage (page 52, first paragraph) where the data moves between stripes/stages ("online reconfiguration") or remains in the stage while the stages move between stripes ("striped reconfiguration") (page 51, figure 5; page 53, figure 9; etc.)]**.

Abramovici and Schmit are analogous art, as they are within the same field of endeavor, namely reconfigurable processing units.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the striped/online reconfiguration of pipelined portions of the FPGA, as taught by Schmit, in each of the FPGAs of the paged reconfiguration system taught by Abramovici.

Because both Abramovici and Schmit teach reconfiguring FPGAs for processing instructions, it would have been obvious to one of ordinary skill in the art to use the striped/online reconfiguration of pipelined portions of the FPGA, as taught by Schmit, in each of the FPGAs of the paged reconfiguration system taught by Abramovici, to achieve the predictable result of providing pipelined execution within pages (when

advantageous to do so) or to allow multiple configurations to be run on the same FPGA simultaneously, thus increasing the system throughput. Schmit provides further motivation as **[by allowing reconfiguration of portions of an FPGA while the remaining portions continue execution, the performance of applications is improved, and pipelined applications can approach the theoretical maximum attainable performance (page 47, abstract; etc.) while also allowing for smaller configuration busses, using fewer of the valuable interconnect resources and decreasing transmission delays (pages 48-49, section 2.4)]**.

As per claim 51, Schmit teaches wherein the first data processing sub-unit is allocated to perform a first operation **[each stripe includes a number of cells (page 54, figure 11), where each cell can function as several things, including an ALU (page 54, section 5.0)]** and the second data processing sub-unit is allocated to perform a second operation **[each stripe includes a number of cells (page 54, figure 11), where each cell can function as several things, including an ALU (page 54, section 5.0)]** and, when the second data processing sub-unit is not involved in performing the second operation, the second data processing sub-unit is reallocated to perform a third operation **[each stripe includes a number of cells (page 54, figure 11), where each cell can function as several things, including an ALU (page 54, section 5.0), where the stripes are reconfigured one stage at a time (page 51, figure 5; page 53, figure 9; etc.), such as shown in the bottom stripe of figure 9b, etc.]**.

Response to Arguments

8. Applicant's arguments with respect to claims 50-51 have been considered but are moot in view of the new ground(s) of rejection.

Abramovici teaches a system of paged configuration of connected FPGAs, controlled by a central page manager, while Schmit teaches striped reconfiguration of individual FPGAs for pipelined operations.

Conclusion

9. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 1-49 are cancelled; claims 50 and 51 are rejected.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Trimberger et al. (A Time-Multiplexed FPGA, 1997, pages 22-28) -- discloses a FPGA system, similar to that disclosed by Schmit, which uses micro registers to pass data between stages.

b. Serrano (US 2006/0126454) -- discloses processing for a demodulator, including a loop filter and positive/negative peak determination.

c. Naoi (US 2003/0200237) -- discloses a pipeline of programmable arithmetic logic units that can be controlled individually or operated together and work in a cascade fashion.

d. Vorbach (US 2006/0248317) - teaches a reconfigurable circuit which can be divided dynamically to perform given operations.

e. Vorbach (US 7,003,660) -- discloses pipelining configurable processing units.

f. Pickett (US 4,942,319) -- discloses multiple programmable pages configured into a programmable array, including moving signals between.

11. The examiner requests, in response to this Office action, that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

12. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE D. GIROUX whose telephone number is (571)272-9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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